

10/730,201

PATENTAMENDMENT A (IN RESPONSE TO PAPER NO. 20040920
(OFFICE ACTION DATED SEPT. 27, 2004))SPECIFICATION

At pages 2-3, please delete paragraph 0006 as follows:

~~[0006] In accordance with another embodiment of the presently claimed invention, a MOS bandgap voltage reference circuit includes MOS current source circuitry, parasitic substrate transistor circuitry, a resistance, amplifier circuitry, resistive circuitry and a plurality of dummy transistors. The MOS current source circuitry includes a control terminal and first, second, third and fourth output terminals, and is responsive to a control signal by providing an output voltage via the first output terminal, substantially equal first and second source currents via the second and third output terminals, and first and second source voltages via the third and fourth output terminals. First parasitic substrate transistor circuitry is coupled to the second output terminal and includes first base, emitter and collector terminals and a first emitter area. Second parasitic substrate transistor circuitry is coupled to the third output terminal and includes second base, emitter and collector terminals and a second emitter area, wherein the first emitter area is greater than the second emitter area, and one of the second emitter and collector terminals is mutually coupled with a like one of the first emitter and collector terminals. The resistance is coupled between the first and second base terminals. The amplifier circuitry is coupled to the third and fourth output terminals and the control terminal, and is responsive to the first and second source voltages by providing the control signal. The resistive circuitry is coupled to the first output terminal, the second base terminal and the mutually coupled first and second parasitic substrate transistor circuitry terminals. The plurality of dummy transistors includes mutually coupled base terminals coupled to the second base terminal, and mutually coupled emitter terminals and mutually coupled collector terminals coupled to the mutually coupled first and second parasitic substrate transistor circuitry terminals.~~

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